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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,867	02/19/2004	Kazuya Hizawa	OKI.390C	1983

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EXAMINER	
NOVACEK, CHRISTY L	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 05/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/780,867	HIZAWA, KAZUYA	
	Examiner	Art Unit	
	Christy L. Novacek	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3-10 and 21-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3-10 and 21-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/283,189.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the amendment and request for continued examination filed May 5, 2006.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 5, 2006 has been entered.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 3-10, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Itonaga (US 20020061639, previously cited) in view of Yu et al. (US 20030029715, previously cited).

Regarding claim 21, Itonaga discloses preparing a substrate (1) having a silicon region (7), forming a metallic layer (8) of a first thickness on the silicon region by a sputtering method, forming a protective layer (9) on the metallic layer such that the protective layer has a second thickness that is greater than the first thickness, forming a metallic silicide layer (10a/10b/10c) in an interface between the silicon region and the metallic layer under the protective layer by a first heat treatment, such that the metallic silicide layer has a high resistance crystalline structure,

removing the protective layer, and subjecting the metallic silicide layer to a second heat treatment after removing the protective layer so that the metallic silicide layer has a low resistance crystalline structure (para. 0066-0138). Because the protective layer of Itonaga is made of the same material (titanium-nitride) and because it is made to be thicker than the metallic layer, it appears that the protective layer of Itonaga inherently possesses the function of protecting the metallic layer from a surrounding atmosphere. See *In re Swinehart*, 439 F.2d 210, 212-13, 169 USPQ 226, 229 (CCPA 1971) "where the Patent Office has reason to believe that a functional limitation asserted to be critical for establishing novelty in the claimed subject matter may, in fact, be an inherent characteristic of the prior art, it possesses the authority to require the applicant to prove that the subject matter shown to be in the prior art does not possess the characteristics relied on "); and *In re Fitzgerald*, 619 F.2d 67, 205 USPQ 594 (CCPA 1980) (a case indicating that the burden of proof can be shifted to the applicant to show that the subject matter of the prior art does not possess the characteristic relied on whether the rejection is based on inherency under 35 U.S.C. 102 or obviousness under 35 U.S.C. 103).

Further regarding claim 21, although Itonaga discloses sputtering the metallic layer onto the substrate, Itonaga does not disclose any particular sputtering method. Like Itonaga, Yu discloses a process for sputtering a refractory metal layer onto the source/drain regions of a silicon substrate and heat-treating the metal layer to react with the silicon substrate to form a metal silicide layer (para. 0093-0094). Yu discloses a silicide-forming process that advantageously reduces process complexity, while improving processing efficiency and throughput (para. 0011). The process taught by Yu involves the steps of heating the substrate at a predetermined temperature, forming the metallic layer on the silicon region of the heated

substrate by a straight sputtering method so as to sputter straightly to the silicon region, and forming a metallic silicide layer in an interface between the silicon region and the metallic layer by a heat treatment (para. 0066-0080). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the sputtering process taught by Yu to form the metallic layer of Itonaga because Itonaga discloses using a sputtering process to form the layer and because Yu teaches that his sputtering process advantageously reduces process complexity, while improving processing efficiency and throughput.

Itonaga discloses that the substrate can be an SOI (silicon-on-insulator) substrate. As is well known in the art, a silicon-on-insulator substrate includes a substrate, an insulating film on the substrate and a silicon layer on the insulating film. At the time of the invention, it would have been obvious to one of ordinary skill in the art to form the SOI substrate of Itonaga by preparing a substrate, forming an insulating film on the substrate and forming a silicon layer on the insulating film because this is the conventional SOI structure and SOI substrates are well known in the art.

Itonaga does not disclose the sheet resistance of the metallic silicide layer. However, because the metallic silicide layer of Itonaga is made of the same material (titanium silicide) and because it is created in the same way (two annealing steps), it appears that the metallic silicide layer of Itonaga inherently possesses the function of having a sheet resistance of about 10 ohms/sq. Furthermore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use routine experimentation to determine an appropriate resistance value for the metallic silicide layer of Itonaga depending upon the amount of silicon layer

consumed in the silicide-formation process and the temperature at which the annealing takes place.

Regarding claim 3, Yu discloses that the predetermined temperature can be in the range of 10°C-500°C (para. 0068).

Regarding claim 4, Yu discloses that the metallic layer can be formed by a long-throw or collimate sputtering method (para. 0028, 0031, 0032, 0035, 0041, 0042, 0058).

Regarding claim 5, Itonaga discloses that the metallic layer can be cobalt or titanium (para. 0138).

Regarding claim 6, Itonaga discloses that the depth of the silicon region is larger than the first thickness of the metallic layer (Fig. 1B).

Regarding claim 7, Itonaga discloses that the protective layer can be made of titanium-nitride (para. 0069).

Regarding claim 8, Itonaga discloses that the first thickness of the metallic layer is 8nm (para. 0069).

Regarding claim 9, Itonaga fails to disclose that the second thickness of the protective layer is equal to or more than 30nm. At the time of the invention, it would have been obvious to one of ordinary skill in the art to use routine experimentation to determine an appropriate thickness of which to form the protective layer of Itonaga, depending upon the materials being used for the metallic layer and the protection layer and the atmospheric conditions of the deposition and annealing processes, because such variables of art recognized importance are subject to routine experimentation and discovery of an optimum value for such variables is obvious. See *In re Aller*, 105 USPQ 233 (CCPA 1955). Furthermore, Applicant's specification

contains no disclosure of either the critical nature of the claimed dimension or any unexpected results arising therefrom.

Regarding claim 10, Itonaga discloses a source region and a drain region (7) of a MOS transistor are formed in the silicon region wherein the metallic silicide layer is formed (para. 0066).

Regarding claim 22, Itonaga discloses that the MOS transistor includes a polysilicon gate (4), forming a metallic layer on the gate, and forming the metallic silicide layer in an interface between the gate and the metallic layer (Fig. 1C; para. 0066).

Claims 23-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Itonaga (US 20020061639, previously cited) in view of Yu et al. (US 20030029715, previously cited) and Wu (US 6,534,405).

Regarding claim 23, Itonaga discloses preparing a substrate (1) having a silicon region (7), forming a metallic layer (8) of a first thickness on the silicon region by a sputtering method, forming a protective layer (9) on the metallic layer, forming a first metallic silicide layer (10a/10b/10c) under the protective layer by a first heat treatment, such that the metallic silicide layer has a high resistance crystalline structure, removing the protective layer, and subjecting the metallic silicide layer to a second heat treatment after removing the protective layer so that the metallic silicide layer has a low resistance crystalline structure (para. 0066-0138). Although Itonaga discloses sputtering the metallic layer onto the substrate, Itonaga does not disclose any particular sputtering method. Like Itonaga, Yu discloses a process for sputtering a refractory metal layer onto the source/drain regions of a silicon substrate and heat-treating the metal layer to react with the silicon substrate to form a metal silicide layer (para. 0093-0094). Yu discloses a

silicide-forming process that advantageously reduces process complexity, while improving processing efficiency and throughput (para. 0011). The process taught by Yu involves the steps of heating the substrate at a predetermined temperature, forming the metallic layer on the silicon region of the heated substrate by a straight sputtering method so as to sputter straightly to the silicon region, and forming a metallic silicide layer in an interface between the silicon region and the metallic layer by a heat treatment (para. 0066-0080). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the sputtering process taught by Yu to form the metallic layer of Itonaga because Itonaga discloses using a sputtering process to form the layer and because Yu teaches that his sputtering process advantageously reduces process complexity, while improving processing efficiency and throughput.

Itonaga discloses that the substrate can be an SOI (silicon-on-insulator) substrate. As is well known in the art, a silicon-on-insulator substrate includes a substrate, an insulating film on the substrate and a silicon layer on the insulating film. At the time of the invention, it would have been obvious to one of ordinary skill in the art to form the SOI substrate of Itonaga by preparing a substrate, forming an insulating film on the substrate and forming a silicon layer on the insulating film because this is the conventional SOI structure and SOI substrates are well known in the art.

Itonaga does not disclose the thickness of the second metallic silicide layer. Like Itonaga, Wu discloses a method of forming a metallic silicide layer on silicon source/drain regions of a transistor. Wu states that the metallic silicide layer can successfully reduce the resistance of the source/drain regions when it has a thickness of 100-600 Angstroms (10-60 nm). Wu teaches that it is desirable to keep the thickness of the metallic silicide layer as thin as

possible in order to reduce the consumption of the source/drain regions (col. 4, ln. 61 – col. 5, ln. 21). At the time of the invention, it would have been obvious to one of ordinary skill in the art to form the metallic silicide layer of Itonaga such that it is within the range of 100-600 Angstroms thick because, as is taught by Wu, it is desirable to keep the metallic silicide layer as thin as possible in order to reduce the consumption of the source/drain regions.

Regarding claims 24 and 26, Itonaga discloses that the metallic layer can be cobalt or titanium (para. 0138).

Regarding claim 25, Yu discloses that the predetermined temperature can be in the range of 10°C-500°C (para. 0068).

Regarding claim 27, Itonaga discloses that the first metallic silicide layer is a metal-rich silicide (Ti_2Si) and the second metallic silicide layer is a stoichiometric metal silicide layer ($TiSi_2$) (para. 0071, 0076).

Regarding claim 28, Applicant's specification discloses that the orientation of the metallic layer is a result of the temperature at which the layer is sputtered onto the substrate (Fig. 12). Applicant's specification discloses that at sputtering temperatures of 400°C, the metallic layer will be most likely to have an orientation of a (200) surface (Fig. 12). Yu discloses that the metallic layer is sputtered onto the substrate at a temperature of 10-500°C. Therefore, it appears that the metallic layer of Itonaga, deposited as taught by Yu, would inherently possess the function of having a (200) surface orientation. See *In re Swinehart*, 439 F.2d 210, 212-13, 169 USPQ 226, 229 (CCPA 1971) "where the Patent Office has reason to believe that a functional limitation asserted to be critical for establishing novelty in the claimed subject matter may, in fact, be an inherent characteristic of the prior art, it possesses the authority to require the

applicant to prove that the subject matter shown to be in the prior art does not possess the characteristics relied on "); and *In re Fitzgerald*, 619 F.2d 67, 205 USPQ 594 (CCPA 1980) (a case indicating that the burden of proof can be shifted to the applicant to show that the subject matter of the prior art does not possess the characteristic relied on whether the rejection is based on inherency under 35 U.S.C. 102 or obviousness under 35 U.S.C. 103).

Regarding claim 29, Itonaga discloses that the temperature of the first heat treatment is lower than the temperature of the second heat treatment (para. 0071, 0076).

Claims 30-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Itonaga (US 20020061639, previously cited) in view of Yu et al. (US 20030029715, previously cited) and Liaw (US 6,413,803).

Regarding claim 30, Itonaga discloses preparing a substrate (1) having a silicon region (7), forming a metallic layer (8) of a first thickness on the silicon region by a sputtering method, forming a protective layer (9) on the metallic layer, forming a first metallic silicide layer (10a/10b/10c) under the protective layer by a first heat treatment, such that the metallic silicide layer has a high resistance crystalline structure, removing the protective layer, and subjecting the metallic silicide layer to a second heat treatment after removing the protective layer so that the metallic silicide layer has a low resistance crystalline structure (para. 0066-0138). Although Itonaga discloses sputtering the metallic layer onto the substrate, Itonaga does not disclose any particular sputtering method. Like Itonaga, Yu discloses a process for sputtering a refractory metal layer onto the source/drain regions of a silicon substrate and heat-treating the metal layer to react with the silicon substrate to form a metal silicide layer (para. 0093-0094). Yu discloses a silicide-forming process that advantageously reduces process complexity, while improving

processing efficiency and throughput (para. 0011). The process taught by Yu involves the steps of heating the substrate at a predetermined temperature, forming the metallic layer on the silicon region of the heated substrate by a straight sputtering method so as to sputter straightly to the silicon region, and forming a metallic silicide layer in an interface between the silicon region and the metallic layer by a heat treatment (para. 0066-0080). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the sputtering process taught by Yu to form the metallic layer of Itonaga because Itonaga discloses using a sputtering process to form the layer and because Yu teaches that his sputtering process advantageously reduces process complexity, while improving processing efficiency and throughput.

Itonaga discloses that the substrate can be an SOI (silicon-on-insulator) substrate. As is well known in the art, a silicon-on-insulator substrate includes a substrate, an insulating film on the substrate and a silicon layer on the insulating film. At the time of the invention, it would have been obvious to one of ordinary skill in the art to form the SOI substrate of Itonaga by preparing a substrate, forming an insulating film on the substrate and forming a silicon layer on the insulating film because this is the conventional SOI structure and SOI substrates are well known in the art.

Itonaga discloses that, when the metallic layer is a cobalt layer, the first heat treatment is conducted at a temperature of 400-500°C in a nitrogen gas atmosphere. However, Itonaga also discloses that, instead of cobalt, the metallic layer may be made of titanium. Itonaga does not disclose the temperature of the first heat treatment when the metallic layer is made of titanium. Like Itonaga, Liaw teaches a process of forming a titanium layer on source/drain regions of a substrate, subjecting the substrate to a first heat treatment to form a high resistance titanium

silicide layer on the substrate, and later subjecting the substrate to a second heat treatment to form a low resistance titanium silicide layer on the substrate (col. 4, ln. 29-51). Liaw teaches that the first heat treatment of the titanium layer should be conducted at a temperature of 600-750°C in nitrogen ambient (col. 4, ln. 40-43). At the time of the invention, it would have been obvious to one of ordinary skill in the art to anneal the metallic layer of Itonaga at a temperature of 600-750°C when the metallic layer is titanium because Itonaga does not disclose a temperature of the first heat treatment when the metallic layer is titanium and Liaw teaches that the first heat treatment of titanium should be conducted at a temperature of 600-750°C.

Regarding claim 31, Yu discloses that the predetermined temperature can be in the range of 10°C-500°C (para. 0068).

Regarding claim 32, Itonaga discloses that the metallic layer can be cobalt or titanium (para. 0138).

Regarding claim 33, Itonaga discloses that the first metallic silicide layer is a metal-rich silicide (Ti_2Si) and the second metallic silicide layer is a stoichiometric metal silicide layer ($TiSi_2$) (para. 0071, 0076).

Regarding claim 34, Applicant's specification discloses that the orientation of the metallic layer is a result of the temperature at which the layer is sputtered onto the substrate (Fig. 12). Applicant's specification discloses that at sputtering temperatures of 400°C, the metallic layer will be most likely to have an orientation of a (200) surface (Fig. 12). Yu discloses that the metallic layer is sputtered onto the substrate at a temperature of 10-500°C. Therefore, it appears that the metallic layer of Itonaga, deposited as taught by Yu, would inherently possess the function of having a (200) surface orientation. See *In re Swinehart*, 439 F.2d 210, 212-13, 169

USPQ 226, 229 (CCPA 1971) "where the Patent Office has reason to believe that a functional limitation asserted to be critical for establishing novelty in the claimed subject matter may, in fact, be an inherent characteristic of the prior art, it possesses the authority to require the applicant to prove that the subject matter shown to be in the prior art does not possess the characteristics relied on "); and *In re Fitzgerald*, 619 F.2d 67, 205 USPQ 594 (CCPA 1980) (a case indicating that the burden of proof can be shifted to the applicant to show that the subject matter of the prior art does not possess the characteristic relied on whether the rejection is based on inherency under 35 U.S.C. 102 or obviousness under 35 U.S.C. 103).

Regarding claim 35, Itonaga discloses that the temperature of the first heat treatment is lower than the temperature of the second heat treatment (para. 0071, 0076).

Response to Arguments

Applicant's arguments filed May 5, 2006 have been fully considered but they are not persuasive.

Regarding the rejections of claims 21, 23 and 30, Applicant argues that Itonaga allegedly fails to disclose the specific structure of a silicon-on-insulator substrate. Silicon-on-insulator substrates are well known and conventional in the art. It is well within the ability of someone of ordinary skill in the art to apply the invention of Itonaga to a silicon-on-insulator substrate, especially in view of the fact that Itonaga states that the substrate may be a silicon-on-insulator substrate.

Regarding the rejection of claim 21, Applicant argues that Itonaga allegedly fails to disclose forming the metallic silicide layer such that it has a sheet resistance of about 10 ohms/sq. Because the metallic silicide layer of Itonaga is made of the same material (titanium or

cobalt silicide) and because it is created in the same way (two annealing steps) as the metallic silicide of Applicant, it appears that the metallic silicide layer of Itonaga inherently possesses the function of having a sheet resistance of about 10 ohms/sq.

Regarding the rejection of claim 23, Applicant argues that Itonaga allegedly fails to disclose forming the second metallic silicide layer such that it has a thickness of about 30 nm. Wu discloses that it is desirable to form such a silicide layer such that it has a thickness of only 10-60 nm, so as to reduce the consumption of the source/drain layer. Therefore, it would have been obvious to one of ordinary skill in the art to form the second metallic silicide layer of Itonaga of a thickness of only 10-60 nm.

Regarding the rejection of claim 30, Applicant argues that Itonaga allegedly fails to disclose performing the first heat treatment at a temperature of 750°C. Itonaga discloses that the metallic silicide layer can be made of titanium silicide, but Itonaga does not disclose the temperature of the first heat treatment when the metallic layer is made of titanium. Liaw discloses that a titanium layer needs to be annealed at a temperature of 600-750°C during a first heat treatment in order for the titanium to react with the substrate to form a titanium silicide. Therefore, it would have been obvious to one of ordinary skill in the art to perform the first heat treatment of Itonaga at a temperature of 600-750°C when the metallic layer is made of titanium.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (571) 272-1839. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CLN
May 15, 2006

Zandra V. Smith
Supervisory Patent Examiner
15 May 2006